

VLSI Design

Lecture 8: Wire delay, Switch logic

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Adapted, with modifications, from lecture notes prepared by the
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Topics

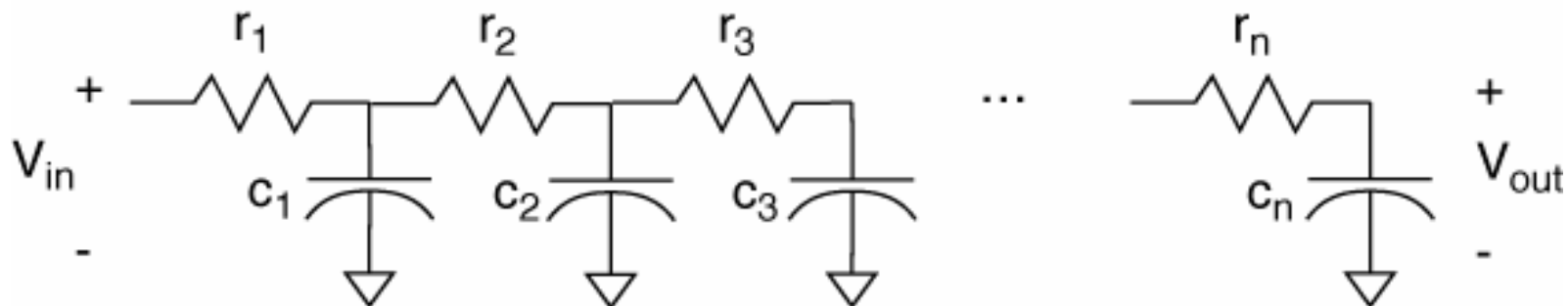
- Wire delay.
- Buffer insertion.
- Crosstalk.
- Inductive interconnect.
- Switch logic.

Wire delay

- Wires have parasitic resistance, capacitance.
- Parasitics start to dominate in deep-submicron wires.
- Distributed RC introduces time of flight along wire into gate-to-gate delay.

RC transmission line

- Assumes that dominant capacitive coupling is to ground, inductance can be ignored.
- Elemental values are r_i , c_i .
 - ❖ All the transmission line section r 's and c 's are identical.



RC Elmore delay

- Can be computed as sum of sections:

$$\delta_E = \sum_{i=1}^n r(n-i)c = 0.5 rcn(n-1)$$

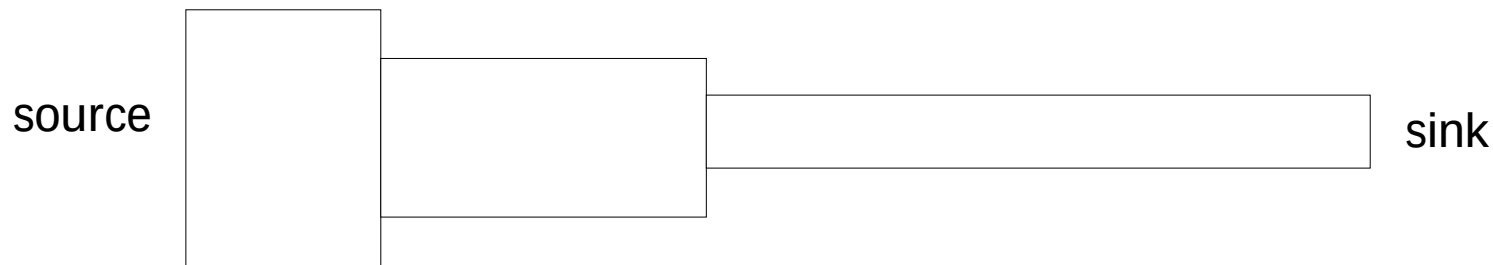
- Resistor r_i must charge all downstream capacitors.
- Delay grows as square of wire length.
- Minimizing rc product minimizes growth of delay with increasing wire length.
 - ❖ Therefore, use metal.

Wire sizing

- Wire length is determined by layout architecture, but we can choose wire width to minimize delay.
- Wire width can vary with distance from driver to adjust the resistance which drives downstream capacitance.

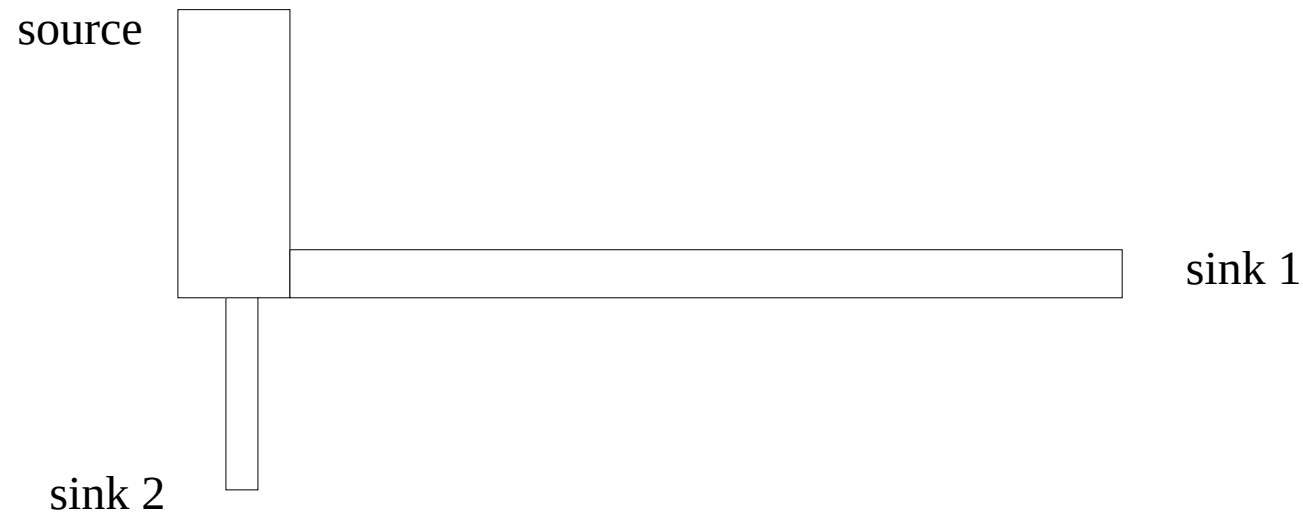
Optimal wiresizing

- Widening the wire reduces the resistance, but increases its capacitance.
- Wire with minimum delay has an exponential taper.
- Optimal tapering improves delay by about 8%.
- Can approximate optimal tapering with a few rectangular segments.



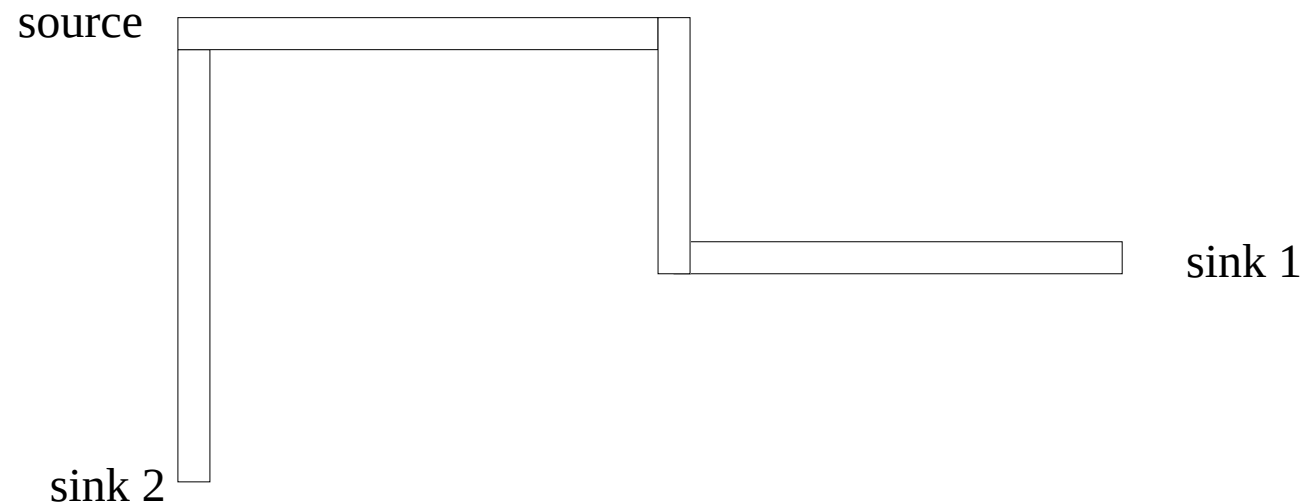
Tapering of wiring trees

Different branches of tree can be set to different lengths to optimize delay.



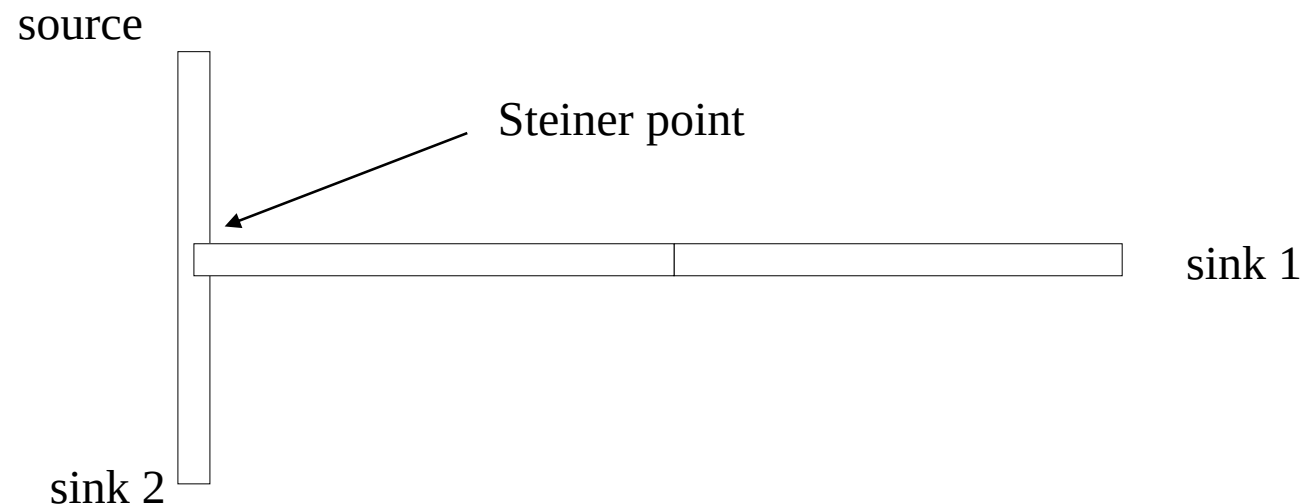
Spanning tree

A spanning tree has segments that go directly between sources and sinks.



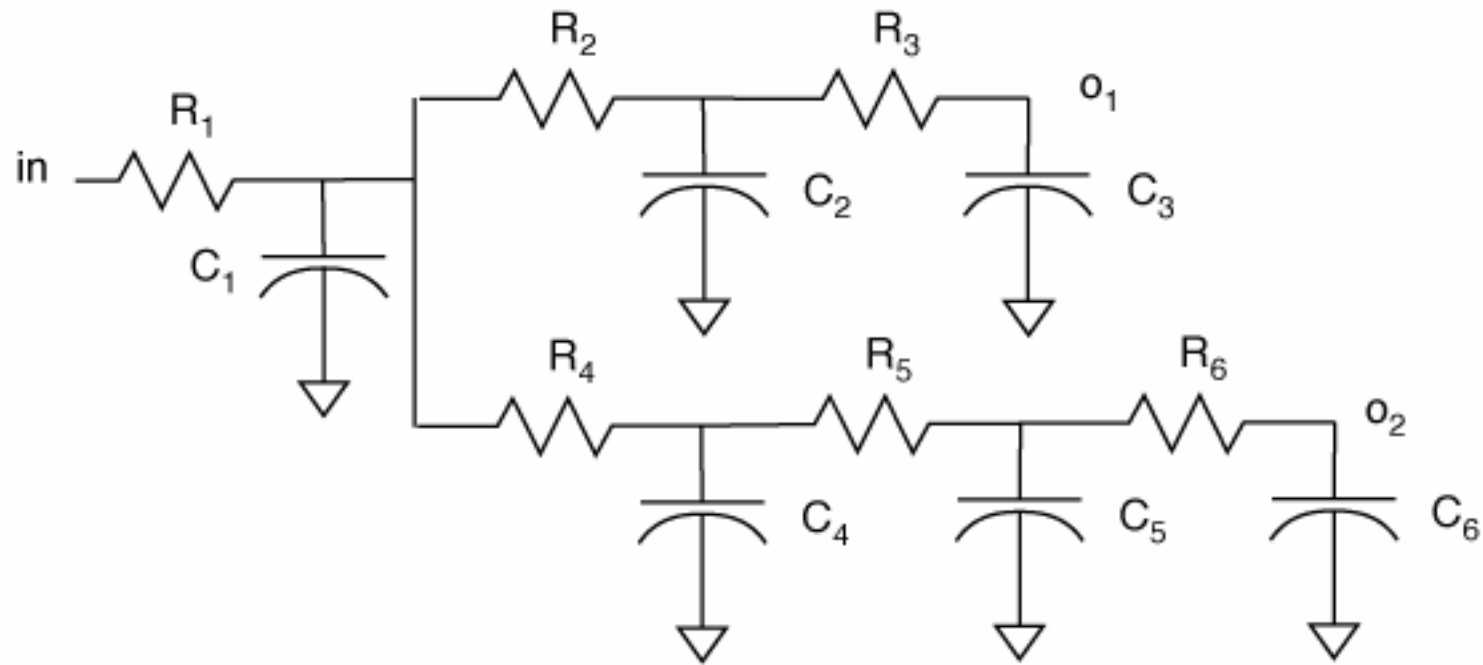
Steiner tree

A Steiner point is an intermediate point for the creation of new branches.



RC trees

Generalization of RC transmission line.



Buffer insertion in RC transmission lines

- Assume RC transmission line.
- Assume R_0 is driver's resistance, C_0 is driver's input capacitance.
- R_{int} and C_{int} are the total resistance and capacitance of the transmission line.
- Want to divide line into k sections of length l . Each buffer is of size h .

Buffer insertion analysis

■ Assume $h = 1$:

$$\diamond k = \sqrt{(0.4 R_{\text{int}} C_{\text{int}})/(0.7 R_0 C_0)}$$

gives the number of repeaters for minimum delay

■ Assume arbitrary h :

$$\diamond k = \sqrt{(0.4 R_{\text{int}} C_{\text{int}})/(0.7 R_0 C_0)}$$

$$\diamond h = \sqrt{(R_0 C_{\text{int}})/(R_{\text{int}} C_0)}$$

$$\diamond T_{50\%} = 2.5 \sqrt{R_0 C_0 R_{\text{int}} C_{\text{int}}}$$

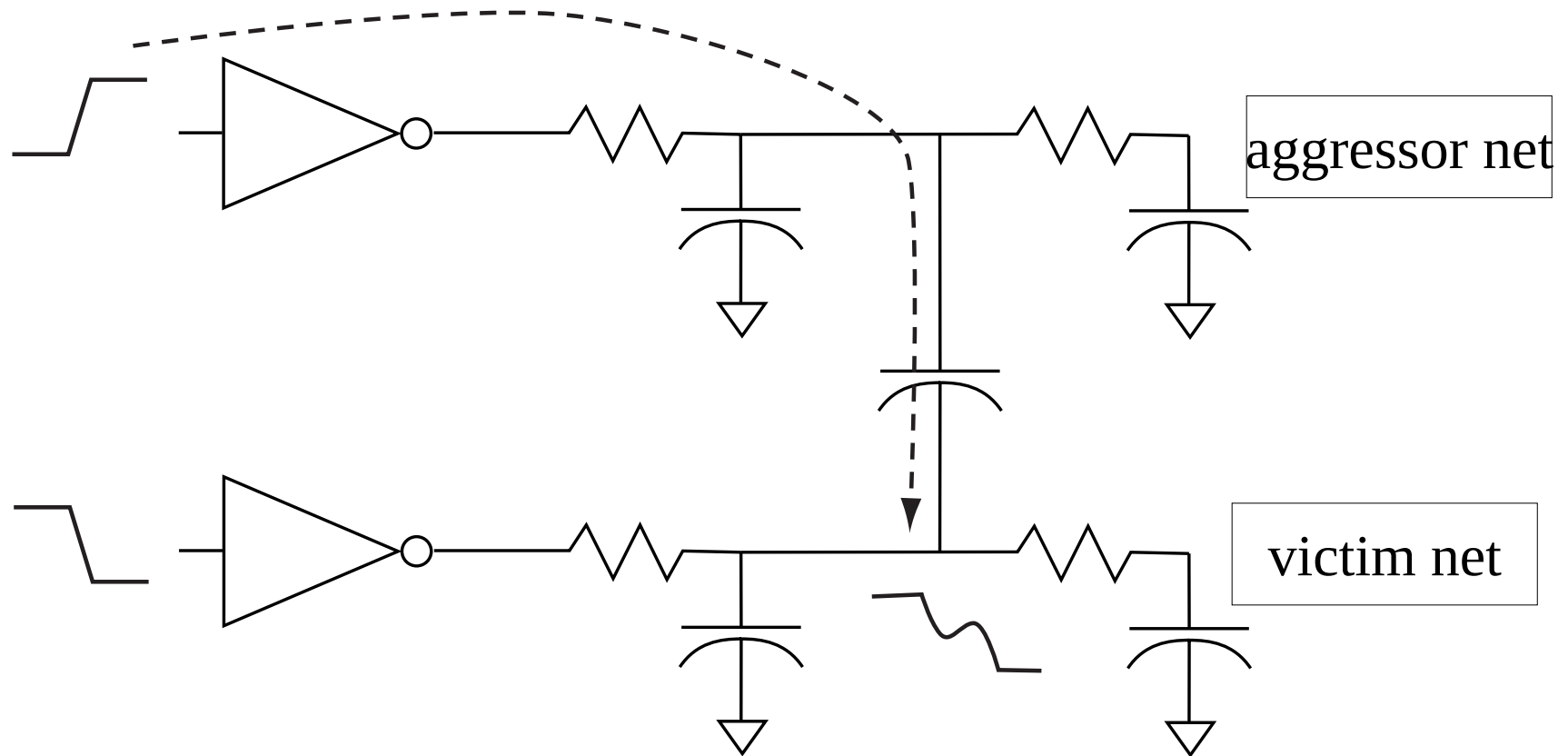
Buffer insertion example

- Minimum-size inverter drives metal 1 wire of $2000 \lambda \times 3 \lambda$.
 - ❖ $R_0 = 3.9 \text{ k}\Omega$, $C_0 = 0.68 \text{ fF}$, $R_{\text{int}} = 53.3 \text{ k}\Omega$, $C_{\text{int}} = 105.1 \text{ fF}$.
- Then
 - ❖ $k = 1.099$.
 - ❖ $H = 106.33$.
 - ❖ $T_{50\%} = 9.64 \text{ E-12}$

RC crosstalk

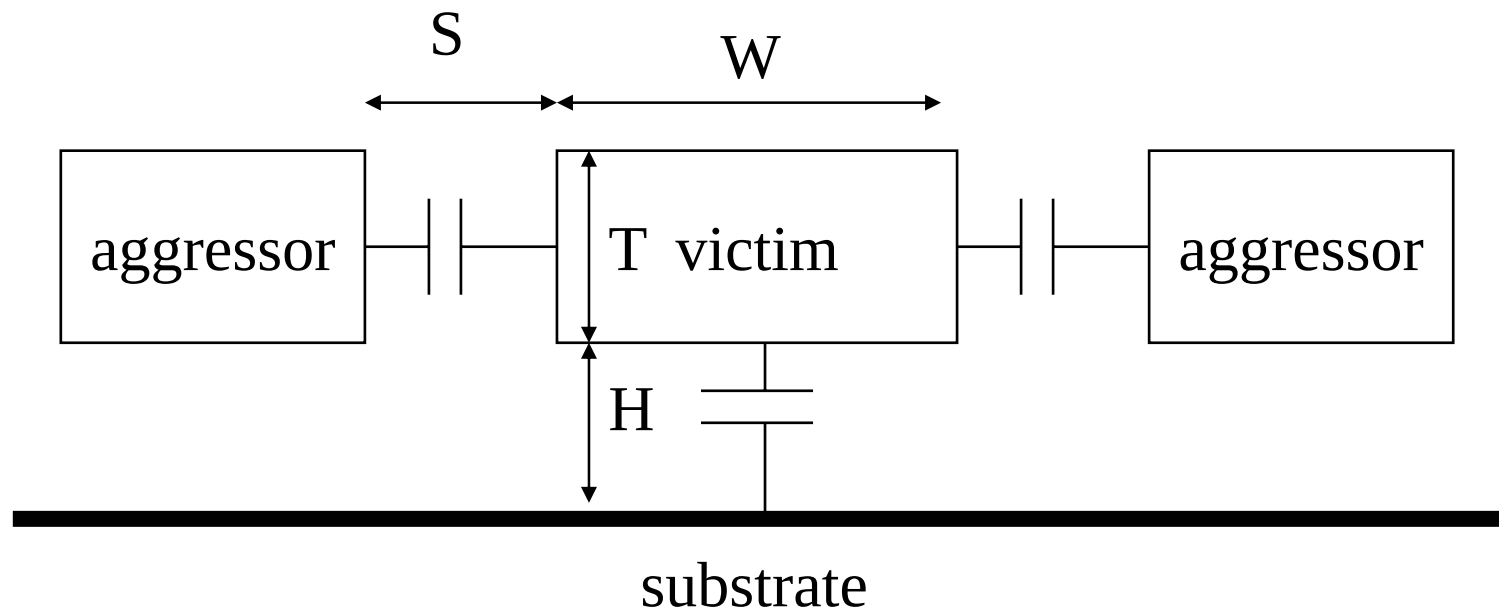
- Crosstalk slows down signals---increases settling noise.
- Two nets in analysis:
 - ❖ aggressor net causes interference;
 - ❖ victim net is interfered with.

Aggressors and victims

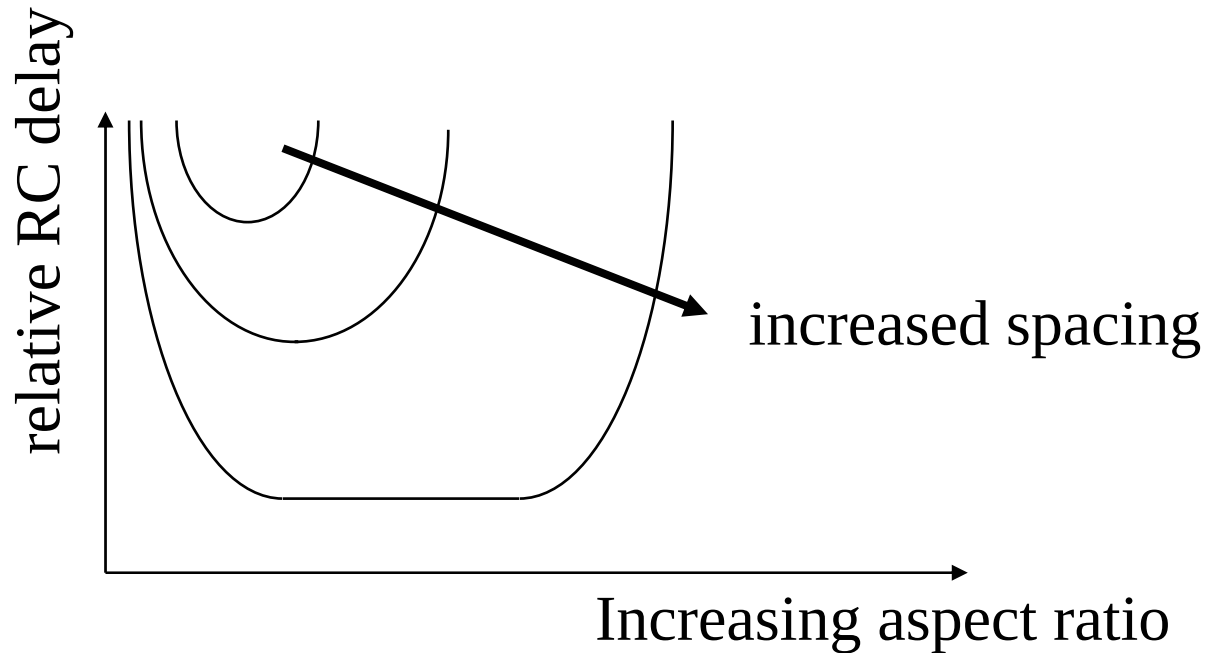


Wire cross-section

- Victim net is surrounded by two aggressors.



Crosstalk delay vs. wire aspect ratio

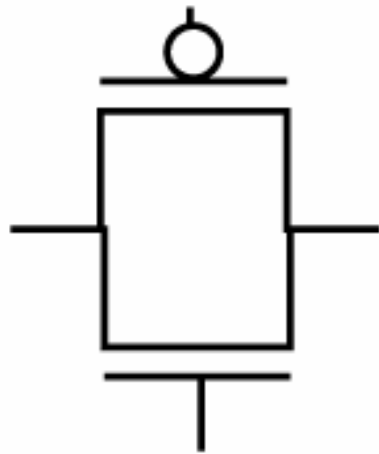


- There is an optimum wire width for any given wire spacing---at bottom of U curve.
- Optimum width increases as spacing between wires increases.

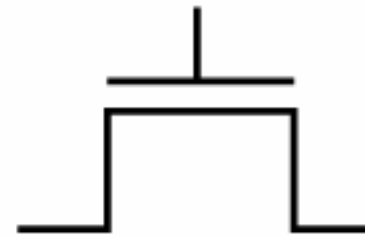
Switch logic

- Can implement Boolean formulas as networks of switches.
- Can build switches from MOS transistors; transmission gates.
- Transmission gates do not amplify but have smaller layouts.

Types of switches



complementary

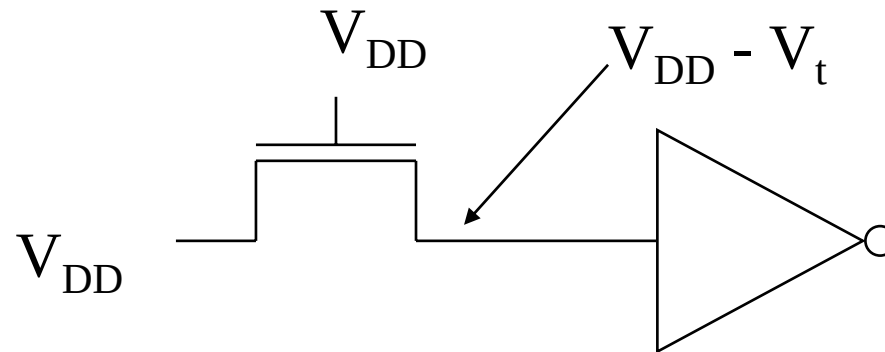


n-type

Behavior of n-type switch

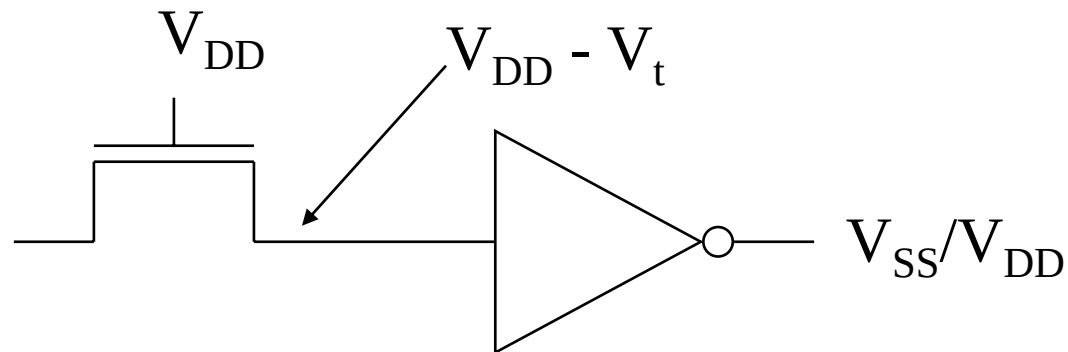
n-type switch has source-drain voltage drop when conducting:

- ❖ conducts logic 0 perfectly;
- ❖ introduces threshold drop into logic 1.



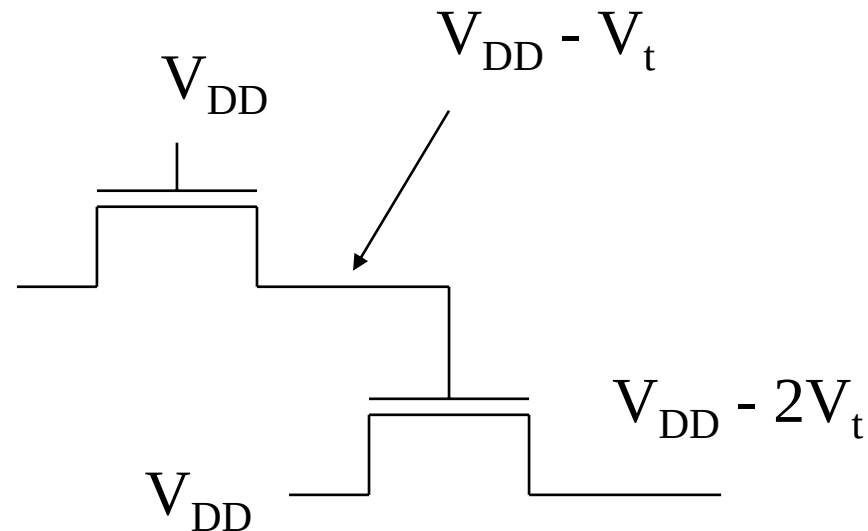
n-type switch driving static logic

Switch underdrives static gate, but gate restores logic levels. Delay is increased.



n-type switch driving switch logic

Voltage drop causes next stage to turn on weakly.



Behavior of complementary switch

- Complementary switch produces full-supply voltages for both logic 0 and logic 1:
 - ❖ n-type transistor conducts logic 0;
 - ❖ p-type transistor conducts logic 1.

Layout characteristics

- Has two source/drain areas compared to one for inverter.
- Doesn't have gate capacitance.

